

What is claimed is:

1 1. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing a polysilicon-bounded test diode, said
4 polysilicon-bounded test diode comprising a diffused first
5 region formed in an upper portion of a second region of a
6 silicon substrate, said second region of an opposite dopant
7 type from said diffused first region, said diffused first
8 region surrounded by a peripheral dielectric isolation and a
9 peripheral polysilicon gate comprising a polysilicon layer
10 over a dielectric layer, said polysilicon gate overlapping a
11 peripheral portion of said diffused first region;

12 stressing said polysilicon-bounded test diode; and

13 monitoring said stressed polysilicon-bounded test diode
14 for spikes in gate current during said stress.

1 2. The method of claim 1, wherein said step of stressing
2 comprises:

3 maintaining said polysilicon-bounded test diode at an
4 elevated temperature;

5 applying ground potential to said polysilicon gate,
6 said second region and said silicon substrate; and
7 applying a reverse bias ramping voltage to between said
8 first and second regions.

1 3. The method of claim 1, wherein

2 said diffused first region has a length of 50 to 100
3 microns and a width of 2 to 10 microns;

4 said polysilicon gate has a width of 0.5 to 1.5
5 microns; and

6 said polysilicon gate overlaps said first diffused
7 region by 0.1 to 0.6 microns.

1 4. The method of claim 2, wherein said ground potential is
2 zero volts and said ramping voltage is ramped from 0 to -6
3 volts and said elevated temperature is 100 to 200 °C.

1 5. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing one or more polysilicon-bounded test diodes,
4 each polysilicon-bounded test diode comprising a diffused
5 first region within an upper portion of a second region of a
6 silicon substrate, said second region of an opposite dopant
7 type from said diffused first region, said diffused first
8 region surrounded by a peripheral dielectric isolation and a
9 peripheral polysilicon gate comprising a polysilicon layer
10 over a dielectric layer, said polysilicon gate overlapping a
11 peripheral portion of said diffused first region;

12 stressing each said polysilicon-bounded test diode;

13 measuring during said stressing, for each said
14 polysilicon-bounded test diode, a current through said first
15 region as a function of a forward bias voltage applied
16 between said first and second regions at at least a
17 predetermined forward bias voltage; and

18 determining the frequency distribution of the slope of
19 said forward bias voltage versus said first region current
20 at said pre-selected forward bias voltage for said one or
21 more polysilicon-bounded test diodes.

1 6. The method of claim 5, wherein said step of stressing
2 comprises:

3 applying ground potential to said polysilicon gate,
4 said second region and said silicon substrate; and
5 applying a forward bias ramping voltage between said
6 diffused first region and said second region.

1 7. The method of claim 5, wherein

2 said diffused first region has a length of 50 to 100
3 microns and a width of 2 to 10 microns;

4 said polysilicon gate has a width of 0.5 to 1.5
5 microns; and

6 said polysilicon gate overlaps said diffused first
7 region by 0.1 to 0.6 microns.

1 8. The method of claim 6, wherein said ground potential is
2 zero volts, said ramping voltage is ramped from 0 to 0.85
3 and said pre-selected voltage is between 0.4 and 0.5 volts.

1 9. The method of claim 5 further comprising:

2 providing one or more STI-bounded reference diodes,
3 said STI-bounded reference diodes each comprising a diffused

4 third region formed in an upper portion of a fourth region
5 of said silicon substrate , said fourth region of an
6 opposite dopant type from said diffused third region, said
7 diffused third region surrounded by a peripheral dielectric
8 isolation;

9 stressing each said STI-bounded reference diode;

10 measuring during said stressing, for each said STI-
11 bounded reference diode, the current through said third
12 diffused region as a function of said forward bias voltage
13 applied between said third diffused region and said fourth
14 regions at at least said predetermined forward bias voltage;

15 determining the frequency distribution of the slope of
16 said forward bias voltage versus said diffused third region
17 current at said pre-selected forward bias voltage for said
18 one or more of STI-bounded reference diodes and

19 comparing said frequency distribution obtained from
20 said STI-bounded reference diodes to said frequency
21 distribution obtained from said polysilicon-bounded
22 reference diodes.

1 10. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing one or more polysilicon-bounded test diodes,
4 each polysilicon-bounded test diode comprising a diffused
5 first region formed in an upper portion of a second region
6 of a silicon substrate, said second region of an opposite
7 dopant type from said diffused first region, said diffused
8 first region surrounded by a peripheral dielectric
9 isolation, a peripheral polysilicon gate comprising a
10 polysilicon layer over a dielectric layer, said polysilicon
11 gate overlapping a peripheral portion of said diffused first
12 region;

13 stressing each said polysilicon-bounded test diode for
14 a pre-determined amount of time; and

15 monitoring, after said stressing, each said
16 polysilicon-bounded test diode for soft breakdown.

1 11. The method of claim 10, wherein said step of stressing
2 comprises:

3 maintaining said polysilicon-bounded diode at an
4 elevated temperature;

5 applying ground potential to said second region, said
6 silicon substrate and said polysilicon gate; and

7 applying a fixed reverse bias voltage to between said
8 first and second regions.

1 12. The method of claim 10, wherein

2 said diffused first region has a length of 50 to 100
3 microns and a width of 2 to 10 microns;

4 said polysilicon gate has a width of 0.5 to 1.5
5 microns; and

6 said polysilicon gate overlaps said diffused region by
7 0.1 to 0.6 microns.

1 13. The method of claim 11, wherein said ground potential is
2 zero volts, said fixed voltage is between -6.3 and less than
3 0 volts, said fixed time is 0.5 hours or more and said
4 elevated temperature is 100 to 200 °C.

1 14. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing a test DRAM, said test DRAM comprising a
4 transfer device having a channel region between first and
5 second P+ regions formed in a N-well in a silicon substrate
6 and a gate formed over said channel region, said second P+
7 region electrically connected to a conductive core of a deep
8 trench capacitor, said substrate acting as a second plate of
9 said deep trench capacitor;

10 stressing said test DRAM; and

11 monitoring said stressed test DRAM for spikes in first
12 P+ region current during said stressing.

1 15. The method of claim 14, wherein said step of stressing
2 comprises:

3 maintaining said test DRAM at an elevated temperature;

4 applying ground potential to said N-well and said first
5 P+ region;

6 applying a voltage to said gate sufficient to turn on
7 said transfer device; and

8 applying a reverse bias ramping voltage to said silicon
9 substrate.

1 16. The method of claim 15, wherein said ground potential is
2 zero volts and said ramping voltage is ramped from 0 to -6
3 volts and said elevated temperature is 100 to 200 °C.

1 17. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing a test DRAM, said test DRAM comprising a
4 transfer device having a channel region between first and
5 second P+ regions formed in a N-well in a silicon substrate
6 and a gate formed over said channel region, said second P+
7 region electrically connected to a conductive core of a deep
8 trench capacitor, said substrate acting as a second plate of
9 said deep trench capacitor;

10 stressing said test DRAM; and

11 monitoring said stressed test DRAM for spikes in gate
12 current during said stressing.

1 18. The method of claim 17, wherein said step of stressing
2 comprises:

3 maintaining said test DRAM at an elevated temperature;

4 applying ground potential to said N-well, said silicon
5 substrate and said gate; and

6 applying a reverse bias ramping voltage to said first
7 P+ region.

1 19. The method of claim 18, wherein said ground potential is
2 zero volts and said ramping voltage is ramped from 0 to -6
3 volts and said elevated temperature is 100 to 200 °C.

1 20. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing a test DRAM, said test DRAM comprising a
4 transfer device comprising a channel region between first
5 and second P+ regions formed in a N-well in a silicon
6 substrate and a gate formed over said channel region, said
7 second P+ region electrically connected to a conductive core
8 of a deep trench capacitor, said substrate acting as a
9 second plate of said deep trench capacitor;

10 stressing said test DRAM;

11 measuring during said stressing, for said test DRAM,
12 the current through said first P+ region as a function of a
13 forward bias voltage applied between said first P+ region
14 and said N-well at at least a pre-selected forward bias
15 voltage; and

16 determining the frequency distribution of the slope of
17 said forward bias voltage versus said first P+ region
18 current at said pre-selected forward bias voltage for said
19 one or more test DRAMs.

1 21. The method of claim 20, wherein said step of stressing
2 comprises:

3 applying ground potential to said N-well and said
4 silicon substrate;

5 applying a voltage to said gate sufficient to turn off
6 said transfer device; and

7 applying a forward bias ramping voltage between said
8 first P+ region and said N-well.

1 22. The method of claim 21, wherein said ground potential is
2 zero volts and said ramping voltage is ramped from 0 to 0.85
3 and said pre-selected voltage is between 0.4 and 0.5 volts.

1 23. The method of claim 20 further comprising:

2 providing one or more reference devices, said reference
3 devices each comprising a third P+ region formed in a N-well
4 in said silicon substrate, said P+ region electrically
5 connected to a conductive core of a deep trench capacitor,
6 said substrate acting as a second plate of said deep trench
7 capacitor;

8 stressing each said reference device identically to
9 said test DRAM;

10 measuring during said stressing, for each said
11 reference device, the current through said third P+ region

12 as a function of said forward bias voltage applied between
13 said third P+ region and said N-well at at least said
14 predetermined forward bias voltage;

15 determining the frequency distribution of the slope of
16 said forward bias voltage versus said P+ region current at
17 said pre-selected forward bias voltage for said one or more
18 of reference devices; and

19 comparing said frequency distribution obtained from
20 said reference devices to said frequency distribution
21 obtained from said test DRAMs.

1 24. A method for detecting semiconductor process stress-
2 induced defects comprising:

3 providing a test DRAM, said test DRAM comprising a
4 transfer device comprising a channel region between first
5 and second P+ regions formed in a N-well in a silicon
6 substrate and a gate formed over said channel region, said
7 second P+ region electrically connected to a conductive core
8 of a deep trench capacitor, said substrate acting as a
9 second plate of said deep trench capacitor;

10 stressing said test DRAM for a pre-determined amount of
11 time; and

12 monitoring, after said stressing, each said test DRAM
13 for soft breakdown.

1 25. The method of claim 24, wherein said step of stressing
2 comprises:

3 maintaining said test DRAM at an elevated temperature;
4 applying ground potential to said first P+ region and
5 said N-well;

6 applying a voltage to said gate sufficient to turn on
7 said transfer device; and

8 applying a fixed reverse bias voltage to said silicon
9 substrate; and

10 wherein said monitoring includes measuring a current
11 through said first P+ diffusion as a function of time.

1 26. The method of claim 25, wherein said ground potential is
2 zero volts, said fixed voltage is between -6.3 and 0 volts,
3 said fixed time is 0.5 hours or more and said elevated
4 temperature is 100 to 200 °C.

1 27. The method of claim 24, wherein said step of stressing
2 comprises:

3 maintaining said test DRAM at an elevated temperature;
4 applying ground potential to said N-well, said gate and
5 said substrate;
6 applying a fixed reverse bias voltage to said first P+
7 region; and

8 wherein said monitoring includes measuring a current
9 through said gate as a function of time.

1 28. The method of claim 27, wherein said ground potential is
2 zero volts, said fixed voltage is between -6.3 and less than

3 0 volts, said fixed time is 0.5 hours or more and said
4 elevated temperature is 100 to 200 °C.

1 29. A method of fabricating an antifuse comprising:

2 providing a silicon substrate having a surface;

3 forming a ring of shallow trench isolation having an
4 inner and an outer perimeter in said substrate extending
5 from said surface of said substrate into said substrate;

6 forming a polysilicon gate overlapping said inner
7 perimeter of said shallow trench isolation on said surface
8 of said substrate, said polysilicon gate comprising a
9 dielectric layer between said surface of said substrate and
10 a polysilicon layer, said polysilicon gate having an inner
11 and outer perimeter;

12 damaging said dielectric layer in a region along said
13 inner perimeter of said polysilicon gate with a heavy ion
14 specie implant to lower the breakdown voltage of said
15 damaged dielectric layer in said region compared to the
16 breakdown voltage in undamaged dielectric regions; and

17 forming a diffused region in said silicon substrate
18 within the inner perimeter of said shallow trench isolation,
19 said diffused region extending from said surface of said
20 substrate into said substrate a depth not exceeding a depth
21 of said shallow trench isolation.

1 30. The method of claim 29 wherein:

2 said diffused region has a length of 1 to 100 microns
3 and a width of 1 to 10 microns;

4 said polysilicon gate has a width of 0.5 to 1.5
5 microns; and

6 said polysilicon gate overlaps said diffused region by
7 0.1 to 0.6 microns.

1 31. The method of claim 29 wherein said heavy ion specie is
2 selected from the group consisting of germanium ion and
3 arsenic ion.

1 32. The method of claim 29 further comprising forming a
2 diffused-well of opposite polarity doping from said diffused
3 region.

1 33. An antifuse comprising:

2 a silicon substrate having a surface;

3 a ring of shallow trench isolation having an inner and
4 an outer perimeter in said substrate extending from said
5 surface of said substrate into said substrate;

6 a polysilicon gate overlapping said inner perimeter of
7 said shallow trench isolation on said surface of said
8 substrate, said polysilicon gate comprising a dielectric
9 layer between said surface of said substrate and a
10 polysilicon layer, said polysilicon gate having an inner and
11 outer perimeter;

12 a damaged region of said dielectric layer, said damaged
13 region along said inner perimeter of said polysilicon gate,
14 said damaged region damaged with a heavy ion specie implant
15 and having a lower breakdown voltage than undamaged regions
16 of said dielectric layer; and

17 a diffused region in said silicon substrate within the
18 inner perimeter of said shallow trench isolation, said
19 diffused region extending from said surface of said
20 substrate into said substrate a depth not exceeding a depth
21 of said shallow trench isolation.

1 34. The antifuse of claim 33 wherein:

2 said diffused region has a length of 1 to 100 microns
3 and a width of 1 to 10 microns;

4 said polysilicon gate has a width of 0.5 to 1.5
5 microns; and

6 said polysilicon gate overlaps said diffused region by
7 0.1 to 0.6 microns.

1 35. The antifuse of claim 33 wherein said heavy ion specie
2 is selected from the group consisting of germanium ion and
3 arsenic ion.

1 36. The antifuse of claim 33 further comprising a diffused-
2 well of opposite polarity doping from said diffused region.

1 37. The antifuse of claim 33 wherein a programming voltage
2 of said antifuse voltage is dependent upon the area of said
3 damaged region and independent of the area of said antifuse.

1 38. The antifuse of claim 33 wherein a programing voltage of
2 said antifuse is a function of one or more of the group
3 consisting of said heavy ion implant, the thickness of said

4 dielectric layer and a temperature of said antifuse when
5 said programing voltage is applied.

1 39. The antifuse of claim 33 wherein the ratio of a
2 resistance of said dielectric layer prior to application of
3 a programing voltage to a resistance of said dielectric
4 layer following application of said programming voltage is
5 greater than 10^7 .

1 40. The antifuse of claim 33 wherein the area of said
2 antifuse is limited by the minimum critical dimension of the
3 photolithographic system used to fabricate the antifuse.